DETAILED ACTION

1. This communication is responsive to Amendment filed 03/20/2008.

2. Claims 1-44 are pending in this application. Claims 1, 16, 24, 31, 38 and 41 are independent claims. This Office Action is made final.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-44 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claim 1, the newly added limitations "determining a number of parallel…on the determined number" in lines 2-4 are not expressively described in the original specification, particularly the step of determining a number of parallel processing blocks based on a capacity to transmit elements, in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Other independent claims 16, 24, 31, 38 and 41 have the same rejection.

Thus, claims 2-15, 17-23, 25-30, 32-37, 39-40 and 42-44 are also rejected for being dependent on the rejected base claims 1, 16, 24, 31, 38 and 41 respectively.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the newly added limitation "storing as speech compression information data describing the determined value" is unclear as what it is trying to store. For examination purposes, the examiner considers that step as storing the determined value. Other independent claims 16, 24, 31, 38 and 41 have the same rejection.

Thus, claims 2-15, 17-23, 25-30, 32-37, 39-40 and 42-44 are also rejected for being dependent on the rejected base claims 1, 16, 24, 31, 38 and 41 respectively.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1-41 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-41 cite a method, article, and system for searching a set of ratio in accordance with a mathematical algorithm. However, claims 1-41 merely disclose steps/components for searching a set of ratio without disclosing a practical/physical application. Further the claims appear to preempt every substantial practical application of the idea embodied by the claims. Even though, the claims disclose a step of storing, but they fail to explain or address how the speech compression utilizes the determined value. Rather, the claims just merely disclose the step of storing as speech compression information data describing the determined value. Therefore, claims 1-41 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-4, 6-17, and 19-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of de Tremiolles et al. (U.S. 6,748,405).

Re claim 1, the admitted prior art discloses in pages 2-4 a method for searching (e.g. paragraph [0002]), comprising: a set of ratios (e.g. expressions 1-4); computing in processing blocks a set of values derived from a set of ratios, each value of the set computed by a respective processing block (e.g. computing the product terms in either expression 3/4); comparing in the processing blocks the respective computed value

against a predetermined value accessible by the respective processing block (e.g. compare against zero as threshold as seen in expression 3/4); selecting one of the computed value and the predetermined value for a respective processing block that is nearer to an optimum value (e.g. page 4 lines 1-4); and determining which of the selected values among the processing blocks is nearest to the optimum value (e.g. page 4 lines 2-6); and storing as speech compression information data describing the determined value (e.g. paragraph [0004]).

The admitted prior art fails to disclose the steps of determining a number of parallel processing blocks based on a capacity to transmit elements of a set of values derived from a set of ratios; dedicating parallel processing blocks based on the determined number; splitting among the dedicated parallel processing blocks elements of a set of values derived and perform other steps in parallel to determine the final optimum value. However, De Tremiolles et al. disclose in Figures 2 and 4 the step of determining a number of parallel processing blocks based on a capacity to transmit elements of a set of values derived from a set of ratios (e.g. Figures 2A-2B as number of p processing blocks); dedicating parallel processing blocks based on the determined number (e.g. each of dash bock is dedicated for determining a specific function); splitting among parallel processing blocks elements of a set of values (e.g. by step A in Figure 4) and perform other steps in parallel (e.g. Figure 2 and step B to F) to determine the final optimum value (e.g. output of step G in Figure 4).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of determining a number of parallel

processing blocks based on a capacity to transmit elements of a set of values derived from a set of ratios; dedicating parallel processing blocks based on the determined number; splitting among parallel processing blocks elements of a set of values and perform other steps in parallel to determine the final optimum value as seen in De Tremiolles et al.'s invention into the admitted prior art's invention because it would enable to increase/improve the response time by processing in parallel (e.g. col. 1 lines 10-16 and col. 2 lines 63-65).

Re claim 2, the admitted prior art fails to disclose in pages 2-4 splitting among parallel processing blocks elements of a set of values derived form a set of ratios comprises splitting among the parallel processing blocks a set of pre-computed values derived from the set of ratios, each pre-computed value of the set associated with a respective processing block. However, De Tremiolles et al. disclose in Figures 2 and 4 splitting among parallel processing blocks elements of a set of values derived form a set of ratios comprises splitting among the parallel processing blocks a set of pre-computed values derived from the set of ratios, each pre-computed value of the set associated with a respective processing block (e.g. wherein pre-computed value is one of the set of P Numbers as clearly addressed in abstract).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add splitting among parallel processing blocks elements of a set of values derived form a set of ratios comprises splitting among the parallel processing blocks a set of pre-computed values derived from the set of ratios, each pre-computed value of the set associated with a respective processing block as seen

in De Tremiolles et al.'s invention into the admitted prior art's invention because it would enable to increase/improve the response time by processing in parallel (e.g. col. 1 lines 10-16 and col. 2 lines 63-65).

Re claim 3, the admitted prior art further discloses in pages 2-4 the set of values derived from a set of ratio and each value of the set computed by a respective processing block (e.g. expression 3-4 in page 3).

The admitted prior art fails to disclose splitting among parallel processing blocks elements of a set of values comprises computing in parallel processing blocks the set of values. However, De Tremiolles et al. disclose in Figures 2 and 4 splitting among parallel processing blocks elements of a set of values (e.g. by step A in Figure 4) comprises computing in parallel processing blocks the set of values (e.g. Figures 2 and steps B to F).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of splitting among parallel processing blocks elements of a set of values comprises computing in parallel processing blocks the set of values as seen in De Tremiolles et al.'s invention into the admitted prior art's invention because it would enable to increase/improve the response time by processing in parallel (e.g. col. 1 lines 10-16 and col. 2 lines 63-65).

Re claim 4, the admitted prior art further discloses in pages 2-4 computing the set of values derived from the set of ratios comprises creating a ratio of an element at an index of a first buffer to an element at a corresponding index of a second buffer (e.g. page 3).

Re claim 6, the admitted prior art further discloses in pages 2-4 comparing the computed value to the predetermined value comprises comparing the computed ratio to a predetermined ratio (e.g. expressions 3-4 in page 3).

Re claim 7, the admitted prior art further discloses in pages 2-4 comparing the computed ratio to the predetermined ratio further comprises: generating a first product of the numerator of the computed ratio multiplied by the denominator of the predetermined ratio; generating a second product of the numerator of the predetermined ratio multiplied by the denominator of the computed ratio; and determining whether the first product minus the second product is greater than zero (e.g. expression 3 in page 3).

Re claim 8, the admitted prior art further discloses in pages 2-4 selecting one of the computed value and the predetermined value that is nearer to the optimum value comprises selecting the computed value if the first product minus the second product is greater than zero, otherwise selecting the predetermined value (e.g. paragraph [0005]).

Re claim 9, the admitted prior art further discloses in pages 2-4 comparing the computed ratio to the predetermined ratio further comprises: generating a first product of the numerator of the computed ratio multiplied by the denominator of the predetermined ratio; generating a second product of the numerator of the predetermined ratio multiplied by the denominator of the computed ratio; and determining whether the first product minus the second product is less than zero (e.g. expression 4 in page 3).

Re claim 10, the admitted prior art further discloses in pages 2-4 selecting one of the computed value and the predetermined value that is nearer to the optimum value

comprises selecting the computed value if the first product minus the second product is less than zero, otherwise selecting the predetermined value (e.g. paragraph [0005]).

Re claim 11, the admitted prior art further discloses in pages 2-4 comparing the ratio to the predetermined value comprises comparing the ratio to an initial-value ratio for the respective processing block (e.g. wherein the initial-value is the predetermined min or max values in expression 3 or 4 in page 3).

Re claim 12, the admitted prior art further discloses in pages 2-4 comparing the ratio to the predetermined value comprises comparing the ratio to a previously computed ratio determined on a previous iteration by the respective processing block to be nearer to the optimum value than a predetermined value of the previous iteration (e.g. paragraph [0005]).

Re claim 13, the admitted prior art further discloses in pages 2-4 selecting one of the computed value and the predetermined value that is nearer to the optimum value comprises selecting the greater of the computed value and the predetermined value (e.g. paragraph [0005]).

Re claim 14, the admitted prior art further discloses in pages 2-4 the set of values comprises buffer elements obtained from buffers accessible by the respective processing blocks, and wherein selecting one of the computed value and the predetermined value that is nearer to the optimum value comprises: storing as the predetermined value in a storage medium accessible by the respective processing block one of the computed value and the predetermined value that is nearer to the optimum value (e.g. paragraph [0005], particularly first nine lines and it is performed in hardware); and repeating the elements

of computing, comparing, and selecting until all available buffer elements have been accessed (e.g. paragraph [0005], particularly last two lines and it is performed in hardware).

Re claim 15, the admitted prior art further discloses in pages 2-4 determining which of the selected values among the processing blocks is nearest to the optimum value comprises: if there are two selected values, repeating the elements of comparing and selecting in a processing block, with the first selected value as the predetermined value and the second selected value as the computed value (e.g. paragraph [0005], particularly first nine lines); and if there are more than two selected values, repeating in parallel processing blocks the elements of comparing and selecting, with the first selected value as the predetermined value and the second selected value as the computed value for each respective processing block (e.g. paragraph [0005], particularly last two lines).

Re claim 16, it is a medium claim having similar limitations cited in claim 1. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, it is a medium claim having similar limitations cited in claim 4. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 19, it is a medium claim having similar limitations cited in claim 6. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 20, it is a medium claim having similar limitations cited in claim 7. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 21, the admitted prior art further discloses in pages 2-4 content to provide instructions to cause the electronic device to select one of the computed value and the predetermined value that is nearer to the optimum value comprises the content to provide instructions to cause the electronic device to (e.g. paragraph [0005]): if a maximum value is searched for, select the computed value if the first product minus the second product is greater than zero, otherwise selecting the predetermined value (e.g. expression 3 in page 3); and if a minimum value is searched for, select the computed value if the first product minus the second product is less than zero, otherwise selecting the predetermined value (e.g. expression 4 in page 3).

Re claim 22, it is a medium claim having similar limitations cited in claim 11. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 23, it is a medium claim having similar limitations cited in claim 12. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 24, it has similar limitations cited in claim 1. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 25, it has similar limitations cited in claim 2. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 26, the admitted prior art further discloses in pages 2-4 separating the elements into the number of different sets comprises separating the elements into a number of different sets (e.g. as product terms in expression 3 or 4 in page 3), the number determined, at least in part, by a number of separate buffer elements fit simultaneously on a data transfer bus from a memory to the processing units (e.g. inherently).

Re claim 27, the admitted prior art further discloses in pages 2-4 for ratio maximization: computing the first product comprises computing the multiplication of an element of the vector A of numerator elements by a denominator member of the initial value pair (e.g. n_1*d_{max} in expression 3 in page 3); and computing the second product comprises computing the multiplication of an element of the vector B of denominator elements by a numerator member of the initial value pair (e.g. $n_{max}*d_1$ in expression 3 in page 3).

Re claim 28, the admitted prior art further discloses in pages 2-4 vector A comprises a correlation vector and vector B comprises an energy vector (e.g. paragraphs [0002-0005] as actual received signal).

Re claim 29, the admitted prior art further discloses in pages 2-4 for ratio minimization: computing the first product comprises computing the multiplication of an element of the vector A of denominator elements by a numerator member of the initial value pair(e.g. n_1*d_{min} in expression 4 in page 3); and computing the second product comprises computing the multiplication of an element of the vector B of numerator elements by a denominator member of the initial value pair (e.g. $n_{min}*d_1$ in expression 4 in page 3).

Re claim 30, it has similar limitations cited in claim 15. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 15.

Re claim 31, it is an apparatus having similar limitations cited in claim 24. Thus, claim 31 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 32, the admitted prior art discloses in pages 2-4 a memory to store vectors A and B (e.g. in page 3-4), but fails to disclose communicatively coupled with parallel processing units via a direct memory access (DMA) channel. However, the examiner takes an official notice that the DMA channel is well-known in the art at the technology and widely used in many practical applications.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the DMA channel into the admitted prior art's invention because it would enable to increase the transferring throughput.

Re claim 33, it has similar limitations cited in claim 25. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 25.

Re claim 34, it has similar limitations cited in claim 26. Thus, claim 34 is also rejected under the same rationale as cited in the rejection of rejected claim 26.

Re claim 35, the admitted prior art discloses in pages 2-4 the data transfer bus comprises a 64-bit bus, and the elements of vectors A and B comprise 16-bit values (e.g. standard or typical).

Re claim 36, it has similar limitations cited in claim 27. Thus, claim 36 is also rejected under the same rationale as cited in the rejection of rejected claim 27.

Re claim 37, it has similar limitations cited in claim 29. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 29.

Response to Amendment

11. The amendment filed 03/20/2008 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

The newly added limitations "determining a number of parallel…on the determined number" in lines 2-4 in every independent claims1, 16, 24, 31, 38 and 41 are considered as new matter introduce into the original disclosure since the original disclosure does not fully provide the support for the newly added limitations above, particularly the step of determining a number of parallel processing blocks based on a capacity to transmit elements.

Applicant is required to cancel or clearly point-out the support of the new matter in the original specification in the reply to this Office Action.

Response to Arguments

12. Applicant's arguments filed 03/20/2008 have been fully considered but they are not persuasive.

a. The applicant argues in pages 17-18 for claims rejected under 35 U.S.C. 101 that the current amended claim including a step of storing as speech compression information

describing the determined value. Thus, they include a useful, concrete, and tangible result as storing speech compression information.

The examiner respectfully submits that the current amended claims do not disclose the step of storing the speech compression information as alleged by the applicant. At most, the claims disclose an unclear step of storing wherein the speech compression information data **describing** the determined value. It is very unclear directly from the claims as how they would overcome the rejection under 35 U.S.C. 101 since the claims merely disclose a series of mental steps including the step of storing.

b. The applicant argues in pages 18-19 for independent claims that the cited secondary reference by de Tremiolles et al. fails to disclose the newly added limitations "determining a number of parallel…on the determined number" in lines 2-4.

The examiner respectfully submits that even assume the original specification fully supports the newly added limitations, the examiner believes the secondary reference by de Tremiolles et al. broadly meet the newly added limitations, particularly Figures 2A-2B. In these Figure, the number of dedicated parallel processors is corresponding to the number of processing blocks which is assigned dynamically as P number.

c. The applicant argues in page 20 for other dependent claims that the cited secondary reference by de Tremiolles et al. fails to disclose both conditionals, as

disclosed through out the dependent claims, (1) comparing a ratio to a previously computed ratio determined on a previous iteration of parallel processing, and/or (2) repeating the elements of comparing and selecting in a processing block if there are two selected values among the processing blocks.

The examiner respectfully submits that the term and/or is considered as alternative form. As clearly addressed in the rejection, secondary reference by de Tremiolles et al. clearly addresses either the condition in the cited reference.

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

d. U.S. Patent No. 6,766,342 to Kechriotis discloses a system and method for computing and unordered Hadamard transform.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Chat C. Do/
Primary Examiner, Art Unit 2193

June 3, 2008